BRIEF DESCRIPTION OF THE DRAWINGS

[0016] Fig. 1 is a simplified block diagram of an integrated circuit according to the present invention.

[0017] Fig. 2 is a simplified block diagram of an integrated circuit according to the present invention for a system on a chip embodiment.

[0018] Fig. 3 is a simplified diagram of a localized charge trapping memory cell that can be used for both code and data flash.

[0019] Fig. 4 is a layout diagram for an array of memory cells, like that of Fig. 3, usable for both code and data flash.

[0020] Figs. 5A-5C illustrate representative program and erase processes for data flash operation of the memory cell of Fig. 3.

TP **[0021]** Figs. 6A-6d illustrate representative program and bit-by-bit erase processes for code flash operation of the memory cell of Fig. 3.

[0022] Fig. 7 is a more detailed diagram of an integrated circuit, including localized charge trapping memory cell arrays configured for code and data storage according to an embodiment of the present invention.

DETAILED DESCRIPTION

[0023] A detailed description of embodiments of the present invention is provided with reference to Figs. 1-7.

[0024] Fig. 1 illustrates the basic concept of the present invention. In particular, an integrated circuit 100 comprises a first memory array 101 adapted for code flash applications, and a second memory array 102 adapted for data flash applications. Peripheral circuits 103 on the integrated circuit include a code and data flash controller which execute first and second operation algorithms which are adapted for the patterns of data usage corresponding with code flash and data flash applications. In preferred embodiments, the memory cells in the first array 101 and the second array 102 have substantially the same structure, while the first and second operation algorithms differ to efficiently support different patterns of data usage within a single integrated circuit device.